In the Claims

1. (currently amended) A multi-loop frequency synthesizer, comprising:

an input terminal for receiving an input reference signal having a frequency f_R;

a fine tune phase locked loop ~~operably~~ coupled to the input terminal and driven by the input reference signal~~, and wherein the fine tune phase locked loop is operable~~ to output a fine tune signal having a frequency $f_R \cdot P$, where P is an integer;

a coarse tune phase locked loop ~~operably~~ coupled to the input terminal and driven by the input reference signal~~, and wherein the coarse tune phase locked loop is operable~~ to output a coarse tune signal having a frequency $f_R \cdot A$, where A is an integer; and

a translation phase locked loop having a unity multiplication factor driven by the fine tune signal, comprising a Gilbert cell double balanced mixer coupled between the coarse tune and the translation phase locked loops, ~~wherein~~ the Gilbert cell mixer combining ~~combines~~ the coarse tune signal and a divided down output signal of the fine tune phase locked loop and coupling ~~couples~~ the mixed signal into the translation phase locked loop~~, whereby~~ to generate an output signal ~~is generated~~ with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal, ~~whereby~~ the low multiplication factor and high bandwidth of the coarse tune loop and the unity multiplication factor of the translation loop reducing ~~reduces~~ the phase noise of the frequency synthesizer.

2. (previously presented) The frequency synthesizer of claim 1, wherein the fine tune phase locked loop includes a divide by D element operable to receive the fine tune signal having a frequency $f_R \cdot P$, where D is an integer, and an output of the divide by D element also comprises an output of the fine tune phase locked loop and provides a signal frequency proportional to $f_R \cdot P/D$ which comprises the divided down signal.

3. (previously presented) The frequency synthesizer of claim 1, wherein the fine tune phase locked loop includes a divide by N_R element operable to receive the input reference signal having a frequency f_R, where N_R is an integer, and a divide by D element operable to receive the fine tune signal having a frequency $f_R \cdot P$, where D is an integer, and an output of the divide by D element also comprises an output of the fine tune phase locked loop and provides a signal frequency proportional to $f_R \cdot P/D \cdot N_R$ which comprises the divided down signal.

4. (previously presented) The frequency synthesizer of claim 3, wherein P, A, D, and N_R are programmable.

5. (previously presented) The frequency synthesizer of claim 3, where A is less than P, and D is greater than N_R.

6. (previously presented) The frequency synthesizer of claim 1, wherein all the elements of the frequency synthesizer are on a single integrated circuit chip.

7. (previously presented) The frequency synthesizer of claim 1, wherein the translation phase locked loop comprises:

a low pass filter coupled to receive the mixed signal output of the Gilbert cell double balanced mixer and to produce a filtered output signal;

a phase detector coupled to receive the divided down fine tune signal and the filtered output signal of the low pass filter and to output a phase detection signal;

a loop filter coupled to receive the phase detection signal and to output a tune voltage;

a voltage controlled oscillator coupled to receive the tune voltage output of the loop filter and generate a signal frequency proportion to the tune voltage; and

a Gilbert cell double balanced mixer coupled between the coarse tune and the translation phase locked loops, wherein the Gilbert cell mixer combines the coarse tune signal and the divided down output signal of the fine tune phase locked loop and couples the mixed signal into the low pass filter of the translation loop, whereby an output signal is generated with a frequency which is proportional to the linear sum of the coarse tune signal and the fine tune signal.

8. (previously presented) The frequency synthesizer of claim 1, wherein the fine tune and coarse tune phase locked loops comprises:

a phase detector operably coupled to receive the input reference signal having a frequency f_R and a divided down feedback signal, and to generate a phase detection signal;

a loop filter operably coupled to receive the phase detection signal and output a tune voltage ;

an oscillator operably coupled to the loop filter to receive the tune voltage and generate a signal frequency proportion to the tune voltage; and

a divider operably coupled between an input of the phase detector and the oscillator output which is the phase locked loop output, and operable to generate the divided down feedback signal, which is a lower frequency signal of the oscillator output.

9. (previously presented) The frequency synthesizer of claim 8, wherein the divider within the fine tune and coarse tune phase locked loops comprises:

a dual modulus prescaler operably coupled to receive the phase locked loop output, wherein the dual modulus prescaler comprises a divide by n_M or n_M+1 element, where n_M or n_M+1 is an integer, and generates a divide by n_M or n_M+1 result output from the operation of the elements;

a swallow divider operably coupled to the dual modulus prescaler, wherein the swallow divider comprises a divide by n_S element, where n_S is an integer, and determines a modulation frequency M for the dual modulus prescaler; and

a programmable divide by n_P element operably coupled to the output of the dual modulus prescaler, where n_P is an integer, and wherein the divide by n_P element is operable to divide the dual modulus prescaler output signal frequency by n_P, whereby the divider provides a signal frequency proportional to $(n_M \cdot n_P + n_S)f_{REF}$ or $(n_M+1 \cdot n_P + n_S)f_{REF}$ which comprises the divided down feedback signal.

10. (previously presented) The frequency synthesizer of claim 1, further comprising:

a divide by D element coupled between the fine tune and the translation phase locked loops; and

a divide by N_R element coupled between the input terminal and the fine tune phase locked loop.

11. (previously presented) The frequency synthesizer of claim 3, further comprising a frequency modulation circuit coupled to the fine tune phase locked loop to operate therethrough, whereby the frequency synthesizer outputs a narrow band FM signal modulated by a modulating signal and filtered at the translation PLL, providing broader bandwidths into the microwave frequency ranges.

12. (previously presented) The frequency synthesizer of claim 7, wherein the low pass filter is coupled to receive the output of the Gilbert cell double balanced mixer, comprises elements using a sigma-delta modulation smoothing technique.

13. (previously presented) The frequency synthesizer of claim 1, further comprising:

a first lock detector circuit coupled to the fine tune phase locked loop;

a second lock detector circuit couple to the coarse tune phase locked loop;

an AND gate coupled to receive the outputs of the first and second lock detectors circuits; and

a sweep circuit coupled to receive the logical output of the AND gate, and generate a sweep signal associated with the translation loop VCO, wherein when a lock condition is detected in both the first and second lock detector, the sweep signal is initiated which generates a frequency sweep of the translation loop VCO to establish a translation loop lock condition at the frequency of the upper sideband mixing product.

14. (currently amended) A method of synthesizing a signal from a lower frequency reference signal, comprising:

providing a fine tune phase locked loop having an input terminal and a coarse tune phase locked loop having an input terminal;

inputting a reference signal with a frequency f_R and applying the reference signal to the ~~an~~ input terminals of the ~~a~~ fine tune phase locked loop and the ~~a~~ coarse tune phase locked loop;

multiplying a frequency f_R of the reference signal by a factor P in the fine tune phase locked loop to generate a fine tune signal;

multiplying a frequency f_R of the reference signal by a factor A in the coarse tune phase locked loop to generate a coarse tune signal;

applying the fine tune signal to a translation phase locked loop; and

Gilbert cell double balanced mixer summing the coarse tune signal and a divided down output of the fine tune signal and coupling the mixed signal into the translation phase locked loop to generate an output signal having a higher frequency proportional to $f_RP/D \cdot N_R + A)$.

15. (previously presented) The method of claim 14, further comprising:

dividing the reference signal by a factor N_R prior to applying the reference signal to the fine tune phase locked loop; and

dividing the fine tune signal by a factor D prior to applying the fine tune signal to the translation loop phase locked loop.

16. (previously presented) The method of claim 14, further comprising a lock detection and sweep operation comprising:

applying the fine tune loop phase detector inputs to a fine tune lock detector circuit;

applying the coarse tune loop phase detector inputs to a coarse tune lock detector circuit;

applying the fine and coarse tune lock detector circuit outputs to an AND gate;

logically ANDing the fine and coarse tune lock detector circuit outputs to indicate when both have achieved lock;

applying the AND gate output to a one-shot circuit to generate a pulse;

applying the one-shot pulse to initiate a sweep circuit associated with a loop filter of the translation loop;

generating a ramp waveform within the sweep circuit;

applying the sweep circuit ramp waveform to a VCO of the translation loop;

sweeping the translation loop VCO; and

determining if the translation loop has established a lock condition at an upper sideband mixing product while sweeping the translation loop VCO, wherein when lock has been established, the sweep signal is discontinued and disabled from further one-shot initiation pulses, otherwise continuing the VCO sweep until lock is established or the minimum frequency is achieved, and ending the lock detection and sweep operation.